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A

UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	042390.P9220
First Inventor or Application Identifier	Robert D. Bateman
Title	CACHE HAVING A PRIORITIZED REPLACEMENT TECHNIQUE AND
Express Mail Label No.	EL034438515US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
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1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [Total Pages 20]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]

4. Oath or Declaration [Total Pages 3]
a. [ ] Newly executed (original copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
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JC498 U.S. PTO 09/609567 06/30/00

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ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
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APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

CACHE HAVING A PRIORITIZED REPLACEMENT TECHNIQUE AND METHOD THEREFOR

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"Express Mail" label number EL034438515US

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CACHE HAVING A PRIORITIZED REPLACEMENT TECHNIQUE AND METHOD THEREFOR

BACKGROUND

In order to provide customers with products that have improved capabilities, it may be desirable to improve the performance of the processor within the product so that the product may operate faster or offer new features. One technique to improve the performance of a processor is to include a cache within the core of the processor. A cache may be used to pre-fetch instructions and/or data that the processor is likely to request in upcoming instruction cycles.

When the processor requests an instruction or a piece of data, the request may be compared against a tag array to determine if the data requested is stored in the cache. If a match is found in the tag array, then a cache "hit" has occurred. Accordingly, the stored information or data may then be provided by the cache. If the requested information is not in the cache, then a cache "miss" has occurred and the information may have to be retrieved from other sources.

In some applications, it may be desirable to arrange the cache into sub-regions, commonly referred to as ways. This may provide more efficient use of the cache since portions of the cache may be designated to store more frequently requested information. If a cache miss has occurred, the information is not in one of the ways of the cache. Consequently, the information is retrieved from a slower memory source and stored in one of the ways of the cache. Often, the information is stored in the way that has been least recently used (LRU). However, conventional LRU replacement techniques do not provide any prioritization of the ways. Consequently, the least recently used way may be overwritten with

the new data (e.g., victimized) even though it contains information that may be requested by the processor in the near future.

Thus, there is a continuing need for better ways to improve the efficiency of a cache.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a schematic representation of an embodiment the present invention;

FIG. 2 is a schematic representation of a portion of a cache in accordance with an embodiment the present invention;

FIG. 3 is a flowchart of updating a cache in accordance with an embodiment of the present invention; and

FIG. 4 is a schematic or a circuit that may be used in accordance with an embodiment of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

Some portions of the detailed description which follow are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art.

An algorithm is here, and generally, considered to be a self-consistent sequence of acts or operations leading to a desired result. These include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like. It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing,"

"computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

Embodiments of the present invention may include apparatuses for performing the operations herein. This apparatus may be specially constructed for the desired purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), electrically programmable read-only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions, and capable of being coupled to a computer system bus.

The processes and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the desired method. The desired structure for a variety of these systems will appear from the description below. In addition, embodiments of the present invention are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the invention as described herein.

Note, in this description a "#" symbol is used to indicate the logical complement of a signal. For example, if BL is a logic "1," then BL# is a logic "0," although this invention is not limited to any particular signaling scheme.

Turning to FIG. 1, an embodiment 100 in accordance with the present invention is described in more detail hereinafter. Embodiment 100 may comprise a portable device, such as a mobile communication device (e.g., cell phone), a portable computer, or the like. However, it should be understood that the scope of the present invention is in no way limited to these particular applications.

Embodiment 100 here includes an integrated circuit 10 that may comprise, for example, a processor, a microprocessor, a digital signal processor, a microcontroller, or the like, hereinafter referred to as a processor 110. However, it should be understood that the scope of the present invention is not limited to these examples. Integrated circuit 10 may include a cache controller 55 that may be used to control the operation of a cache 50 and provide processor 110 with the requested information.

For example, processor may provide cache controller 55 with the address of the information requested. Cache controller 55 may provide that address along with various control signals (e.g., lock signals indicating if a way is locked, read signals, cache hit/miss signals, etc.) to determine if the requested information is in cache 50. If the information is in cache 50, it may be provided to processor 110 by cache controller 55. Otherwise, the data may have to be provided from an alternative memory 56 (e.g. a static memory array (SRAM), or the like). It should be understood that the scope of the present invention is not limited to a particular implementation of cache controller 55 or by the presence of a particular auxiliary memory 56. In addition, the scope of the present invention is not limited by the particular techniques used to transfer address or data information in integrated circuit 10. For example,

address and data information may be exchanged between processor 110, cache controller 55, and cache 50 using bi-directional buses, unidirectional buses, or the like.

Referring now to FIG 2., cache 50 may comprise a tag array 20 divided into four ways 21-24 (labeled A-D, respectively). Tag array 20 may be used to store the tag addresses corresponding to the data that is available in cache 50. Cache 50 may also have a data array 30 divided into four ways 31-34 (labeled A-D, respectively). Ways 31-34 may correspond to ways 21-24 of tag array 20. For example, the data stored in way 31 of data array 30 may correspond to the associated addresses in way 21 of tag array 20, although the scope of the present invention is not limited in this respect.

In this particular embodiment, processor 110 (see FIG. 1) may use a thirty-two bit address to request data or instructions (shown in FIG. 2 as an address 15). A portion of the address (e.g., the lower 12 bits of address 15) may be used to select the set within each of ways 21-24 and 31-35, labeled in FIG. 2 as SET_ADDRESS. The remaining portion of address 15 (e.g., the upper 20 bits) may be used to determine if the information requested by the processor is in cache 50, labeled in FIG. 2 as TAG_ADDRESS.

Accordingly, in this particular embodiment, each of ways 21-24 may contain 4k (2^{12}) sets. However, only four sets 121-124 are shown in FIG. 1 for clarity. Similarly, each of ways 31-34 of data array 30 may have 4k sets of data. However, only four sets 131-134 are shown in FIG. 2. A decoder 60 (e.g., a multiplexor) may be used to select the appropriate set 121-124 and 131-134 of ways 21-24 and 31-34, respectively, based on the logical value of the addressed used to request data, namely, SET_ADDRESS.

It should be understood, however, that the scope of the present invention is not limited by the number of ways in a cache, the number of sets or data rows in a way, or by the width of each set in the cache. One skilled in the art will understand how alternative embodiments of

the present invention may be provided by making the appropriate adjustments. In addition, the scope of the present invention is not limited to any particular technique for accessing tag array 20 and data array 30, and is not limited by the width of the address (e.g., address 15) that is used to request data from the cache.

A method for storing data in cache 50 in accordance with an embodiment of the present invention is provided with reference to FIGs. 1-3. When processor 110 (see FIG. 1) requests information from cache 50 it provides an address (e.g., address 15) indicating the location of the information in memory. Cache controller 55 may first determine if the requested information is in cache 50 (e.g., a cache hit) or if the information is not available from cache 50 (e.g., a cache miss), block 301 of FIG. 3.

When integrated circuit 10 begins operating, cache 50 may not contain any information if cache 50 is not initialized before processor 110 begins requesting information. Consequently, the initial requests of information by processor 110 may result in a cache miss until ways 31-34 of cache 50 are loaded with data. Until all of ways 31-34 of data array 30 are stored with data, there may be no reason to overwrite one of the ways 31-34 that already contains data, block 303, although the scope of the present invention is not limited in this respect. Thus, in this particular embodiment the requested data may be stored in one of unused ways 31-34 if one of ways 31-34 is empty, block 304.

However, If a cache miss has occurred and one of ways 31-34 is not available, then one of ways 31-34 may be victimized (e.g., overwritten) to store the information that was recently requested by processor 110. Although the scope of the present invention is not limited in this respect, the new information is stored in the way of cache 50 that is the least recently used (LRU). This may be more efficient for some applications because the other ways may contain information that has been more recently requested by processor 110, and

thus, may be more likely requested by processor 100 in an upcoming instruction cycle.

In this particular embodiment of the present invention, the identity of the least recently used way may be provided, at least in part, to cache controller 55 by the logical valued stored in a Least Recently Used (LRU) array 70 (see FIG. 2). LRU array 70 may comprise LRU registers 71-74 that correspond to the priorities of the sets 131-134 of data array 30, respectively. For example, LRU register 71 may indicate the relative priority of set 131 in ways 31-34 of data array 30.

Although the scope of the present invention is not limited in this respect, LRU registers may comprise six bits that indicate the priority of one of ways 31-34 relative to another of ways 31-34. In this particular embodiment, data array 30 may have four ways, thus, there may be a total six possible combinations of ways that are compared (e.g., way 32 relative to way 31, way 33 relative to way 31, way 33 relative to way 32, way 34 relative to way 33, way 34 relative to way 32, and way 34 relative to way 31). Table 1 is provided to illustrate an example of how the bits of an LRU register 71-74 may be used to indicate the priority of ways 31-34.

LRU Register [#] Bit Number	Represents
LRU Register [5]	Is way 32 more recently used than way 31?
LRU Register [4]	Is way 33 more recently used than way 31?
LRU Register [3]	Is way 33 more recently used than way 32?
LRU Register [2]	Is way 34 more recently used than way 33?
LRU Register [1]	Is way 34 more recently used than way 32?
LRU Register [0]	Is way 34 more recently used than way 31?

Table 1

For example, if the information most recently requested by processor 110 is stored in way 31, then the LRU register bits[5, 4, and 0] may be set to a logical '0' to indicate that none

of these conditions are true since way 31 has been more recently used then ways 32-34. Likewise, if the next request of processor 110 results in information being stored in way 32, then LRU register bits[5] may be set to a logical '1' to indicate the condition is true, and LRU register bits[3 and 1] may be set to a logical '0' to indicate that these conditions are false. Thus, if ways 31-34 are loaded in sequential, ascending order (e.g., way 31 first, way 34 last), then the corresponding LRU register may have a logical value of '111111.' However, it should be understood that the scope of the present invention is not limited to a particular arrangement of representation by LRU registers 71-74. Similarly, the present invention is not limited by the number of bits that are in LRU registers 71-74. In alternative embodiments, the number of bits in LRU registers 71-74 may be changed as desired for caches having more or less than four ways.

Continuing with the example provided above, if the most recent accesses of ways 31-34 had been in sequential, ascending order, then way 31 may be the least recently used way and may be identified to cache controller 55 (FIG. 1) as the way to be used to store the information most recently requested by processor 110, block 305 of FIG. 3. Cache controller 55 may then store the information in the least recently used of ways 31-34, block 306.

Particular embodiments of the present invention provide a programmer with the ability to lock a way of a cache (e.g., ways 31-34) once it has been loaded with information, block 307. This may be desirable to protect a way from being overwritten even if it becomes the least most recently used. For example, one of ways 31-34 may contain information that is not currently being requested by processor 110, but may be requested in the near future. Although the scope of the present invention is not limited in this respect, a user may lock one of ways 31-34 by notifying cache controller 55, block 309. For example, the user may set a bit in a register (e.g., Lock[#]) that is used by cache controller 55 to keep track of which of ways

31-34 may be locked. Register Lock[#] may comprise a bit indicating if ways 31-34 are locked or if they may overwritten upon the occurrence of a cache miss. It should also be understood that in alternative embodiments of the present invention, a user may desire to lock more than one of ways 31-34.

After a set 131-134 of ways 31-34 has been accessed (e.g., either through a cache read or write), the corresponding LRU register 71-74 may be updated to reflect the change in priorities of ways 31-34, bock 310. As shown in FIG. 2, cache 50 may include a LRU update controller 90 that may be used to update the logical value stored in LRU array 70. LRU update controller 90 may receive signals from cache controller 55 that indicate which of ways 31-34 has been accessed. It should also be understood that in alternative embodiments of the present invention one or more of ways 31-34 may locked or unlocked at any point after the particular way has been loaded with data. In this particular embodiment, the highest priority is given to a way (e.g., one of ways 31-34) that is locked, although the scope of the present invention is not limited in this respect. For example, a way that is locked is given higher priority over the most recently accessed way. Thus, LRU update controller 90 may indicate that a locked way is the highest priority (e.g., most recently used) even though it has not been accessed by processor 110 during one of the recent requests for information.

In this particular embodiment, there may be some situations where more than one of ways 31-34 may be locked. If two or more ways 31-34 are locked, LRU update controller 90 may be arranged to assign priority using different techniques (e.g., assign priority by ascending order, descending order, least recently used, etc.). It should also be understood that there may be situations where the most recently used way 31-4 of data array 30 may actually be given the lowest priority in the corresponding LRU register 71-74 if the other arrays are locked.

Table 2 is provided to illustrate one technique for determining the logical value of the bits in LRU register 71-74. In this table, "Way[n]" is used to indicate which of ways 31-34 is the most recently used. "Lock[n]" and "Lock[n]#" are used to indicate which of ways 31-34 are locked or not locked. respectively.

LRU Register [#] Bit Number	Represents
LRU Register [5]	Lock[31] OR (Way[31] AND Lock[32]#)
LRU Register [4]	Lock[32] OR (Way[32] AND Lock[33]#)
LRU Register [3]	Lock[31] OR (Way[31] AND Lock[33]#)
LRU Register [2]	Lock[33] OR (Way[33] AND Lock[34]#)
LRU Register [1]	Lock[32] OR (Way[32] AND Lock[34]#)
LRU Register [0]	Lock[31] OR (Way[31] AND Lock[34]#)

Table 2

FIG. 4 is provided as an example of how the bits of LRU register 71-74 may be updated to reflect a read or write of one of ways 31-34 in cache 50, although the scope of the present invention is not limited to this particular implementation as other techniques, including software, may be used. For example, Table 1 indicates that the fifth bit of LRU register 71-75 (e.g., LRU Register[5]) may be updated if either way 31 or way 32 is the most recently used way of cache 50 or if either of way 31 or way 32 are locked. Accordingly, the appropriate input signals may be used to determine if LRU Register[5] is updated. As indicated in FIG. 4, the update logic may allow for the prioritizing of a locked way higher than a least recently used way. Further, the logic may also prioritize a locked way higher even if is not the most recently used way, although it should be understood that the scope of the present invention is not limited in this respect. In alternative embodiments, is may be desirable to prioritize ways 31-34 in a different order depending on which ones are locked and which is the most recently used.

Referring now to FIGs. 2-3, a request for information from processor 110 to cache 50

may begin by providing the TAG_ADDRESS to a comparator 95. The SET_ADDRESS may be provided to decoder 60 so that the appropriate set 121-124 of tag array 20 are selected. Comparator 90 may then determine if the value stored in the corresponding set 121-124 of ways 21-24 is sufficiently similar to the TAG_ADDRESS. If a match is found, block 302 of FIG. 3, comparator 90 may indicate which of ways 31-34 is a match (e.g., signal HIT_WAY_ID) to allow multiplexor 96 to provide the data stored in the corresponding way 31-34 of data array 30 as the output data (e.g., DATA_OUT). Comparator 95 may also notify LRU update controller 90 of the occurrence of a cache hit, and the identification of the most recently used way 31-34 so that the corresponding LRU register 71-74 of LRU array 70 may be updated.

If the TAG_ADDRESS does not match any of the logical values stored in ways 21-24 of tag array 20, then a cache miss may have occurred. Accordingly, the logical value stored in the corresponding LRU register 71-74 may be provided to cache controller 55 to identify which of ways 31-34 is to be victimized. Cache controller 55 may use control signals (e.g., Write_Way) to enable decoders 97 and 98 to store the most recent TAG_ADDRESS and data in the least recently used way 21-24 and 31-34 of tag array 20 and data array 30. Thereafter, LRU update controller 90 may update the logical value stored in the corresponding LRU Register 71-74.

By now it should be appreciated that particular embodiments of the present invention provides a method by which one or more ways of a cache may be locked so that they are not overwritten with data. Further, particular embodiments of the present invention may prioritize the ways of a cache so that locked ways are given higher priority than the most recently used or accessed ways. This may improve the efficiency of a cache by permitting a user to protect some of the data store in the cache while using a lest recently used storage technique for the

remaining ways. Accordingly, the number of cache hits may be increased and the operational performance of a processor (e.g., processor 110) may be improved.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. For example, in alternative embodiments it may be desirable to prioritize a locked way lower than the most recently used way. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

Claims:

1. A method for storing data in a cache comprising:

prioritizing a locked way of the cache higher than a recently used way.

2. The method of claim 1, further comprising storing data in the recently used way.

3. The method of claim 1, further comprising:

prioritizing the locked way higher than a least recently used way; and

storing data in the least recently used way.

4. The method of claim 1, further comprising locking at least one way of the cache to provide the locked way.

5. The method of claim 1, further comprising reading data from a way of the cache prior to prioritizing the locked way, the way being the recently used way.

6. The method of claim 1, wherein prioritizing the locked way includes setting a bit in a register.

7. The method of claim 1, further comprising setting a bit in a register to indicate priority of the recently used way.

8. The method of claim 1, further comprising writing data to a way of the cache prior to

prioritizing the locked way, the way being the recently used way.

9. The method of claim 1, further comprising:

locking a first way of the cache to provide the locked way; and

locking a second way of the cache to provide an additional locked way.

10. The method of claim 9, further comprising prioritizing the locked way higher than the additional locked way.

11. The method of claim 9, further comprising:

setting a first bit in a register to indicate priority of the locked way; and

setting a second bit in a register to indicate priority of the additional locked way.

12. The method of claim 11, further comprising setting a third bit in a register to indicate priority of the recently used way.

13. A method comprising:

locking a first way of a cache;

accessing a second way of the cache;

accessing a third way of the cache; and

writing data to the second way of the cache.

14. The method of claim 14, wherein locking the first way includes setting a bit in a register to indicate the priority of the first way.

15. The method of claim 14, wherein writing data to the second way occurs if the second way has been accessed more recently than the first way.

16. The method of claim 16, wherein writing data to the second way occurs if the second way has been accessed more recently than the third way.

17. An apparatus comprising a cache having a first way and a second way, the apparatus comprising:

a circuit adapted to write data to the first way if the first way has been accessed more recently than the second way.

18. The apparatus of claim 18, wherein the circuit if further adapted to lock the second way.

19. The apparatus of claim 18, further comprising a memory location adapted to indicate the priority of the first way and the second way.

20. An article comprising:

a machine readable storage medium having stored thereon instructions capable of being executed by a data processing platform, said instructions being adapted to prioritize a locked way of a cache higher than a least recently used way of the cache.

21. The machine readable storage medium of claim 21, wherein said instructions are further adapted to set a bit in a memory location to indicate the priority of the locked way and the least recently used way.

22. The machine readable storage medium of claim 22, wherein said instructions are further adapted to store data in the least recently used way.

CACHE HAVING A PRIORITIZED REPLACEMENT TECHNIQUE AND METHOD THEREFOR

Abstract

Briefly, in accordance with one embodiment of the invention, a method by which one or more ways of a cache may be locked so that they are not overwritten with data. Further, the ways of a cache that are locked may be given higher priority than the most recently used or accessed ways.

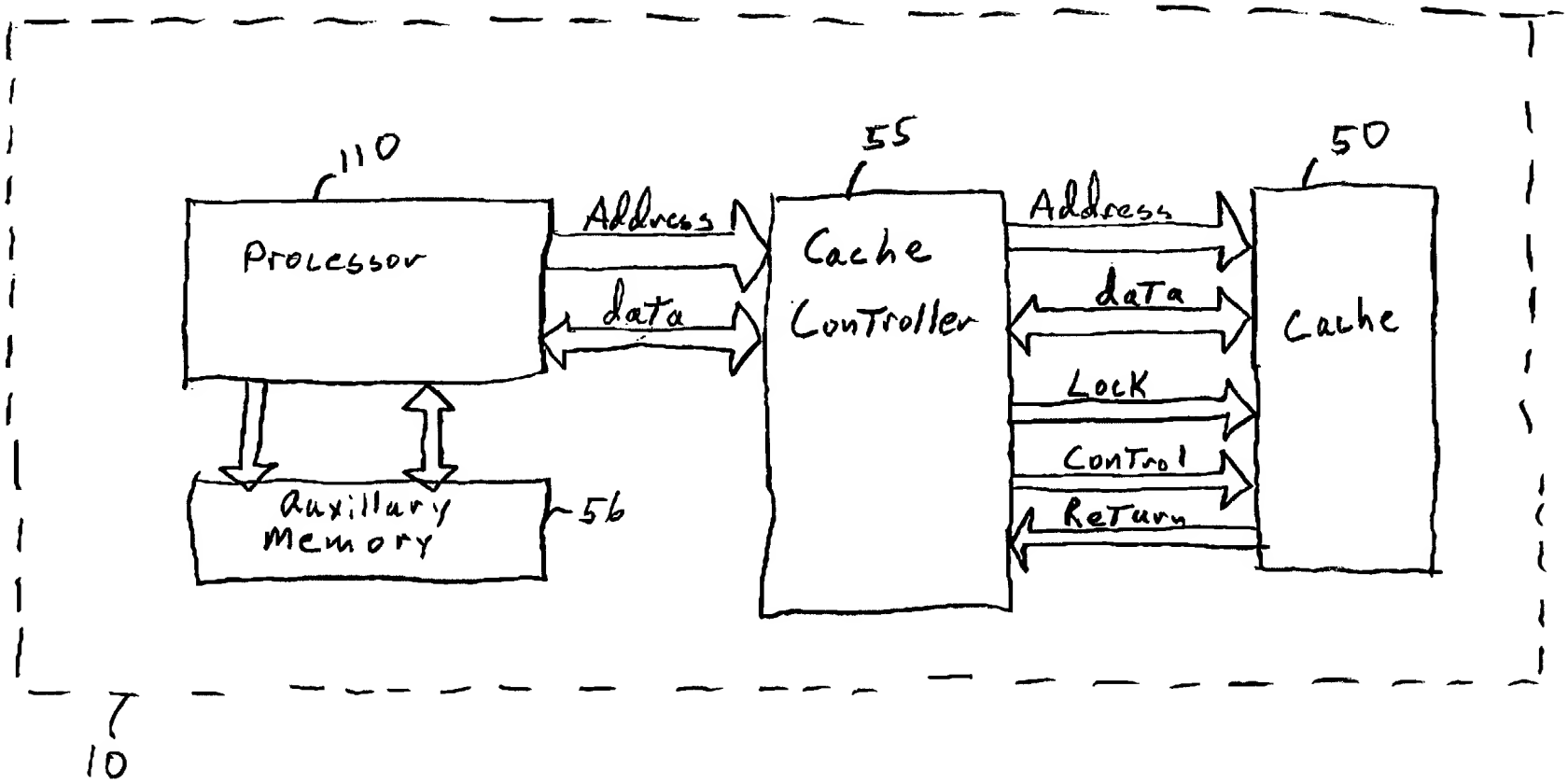

FIG. 1

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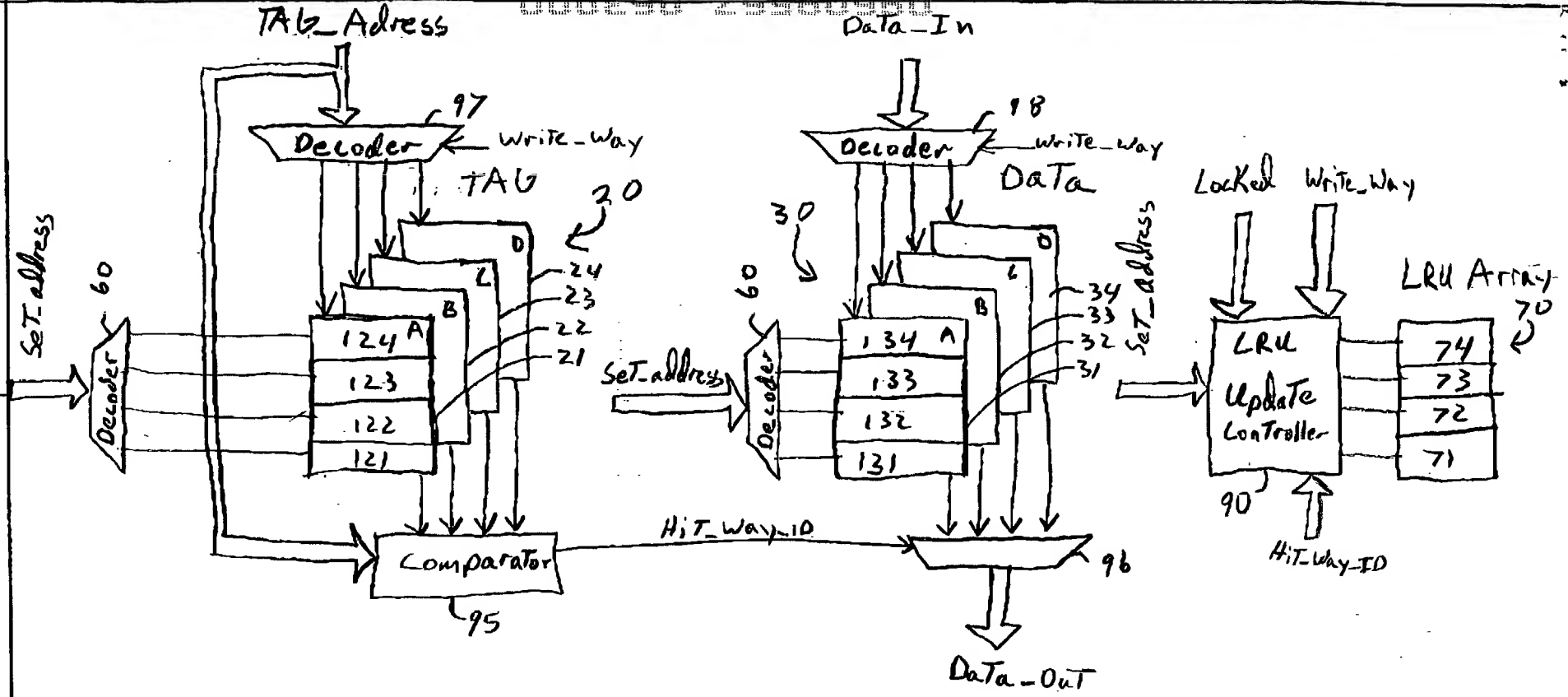

50

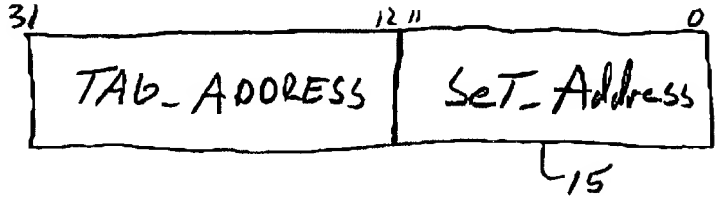

FIG. 2

42390.P9220

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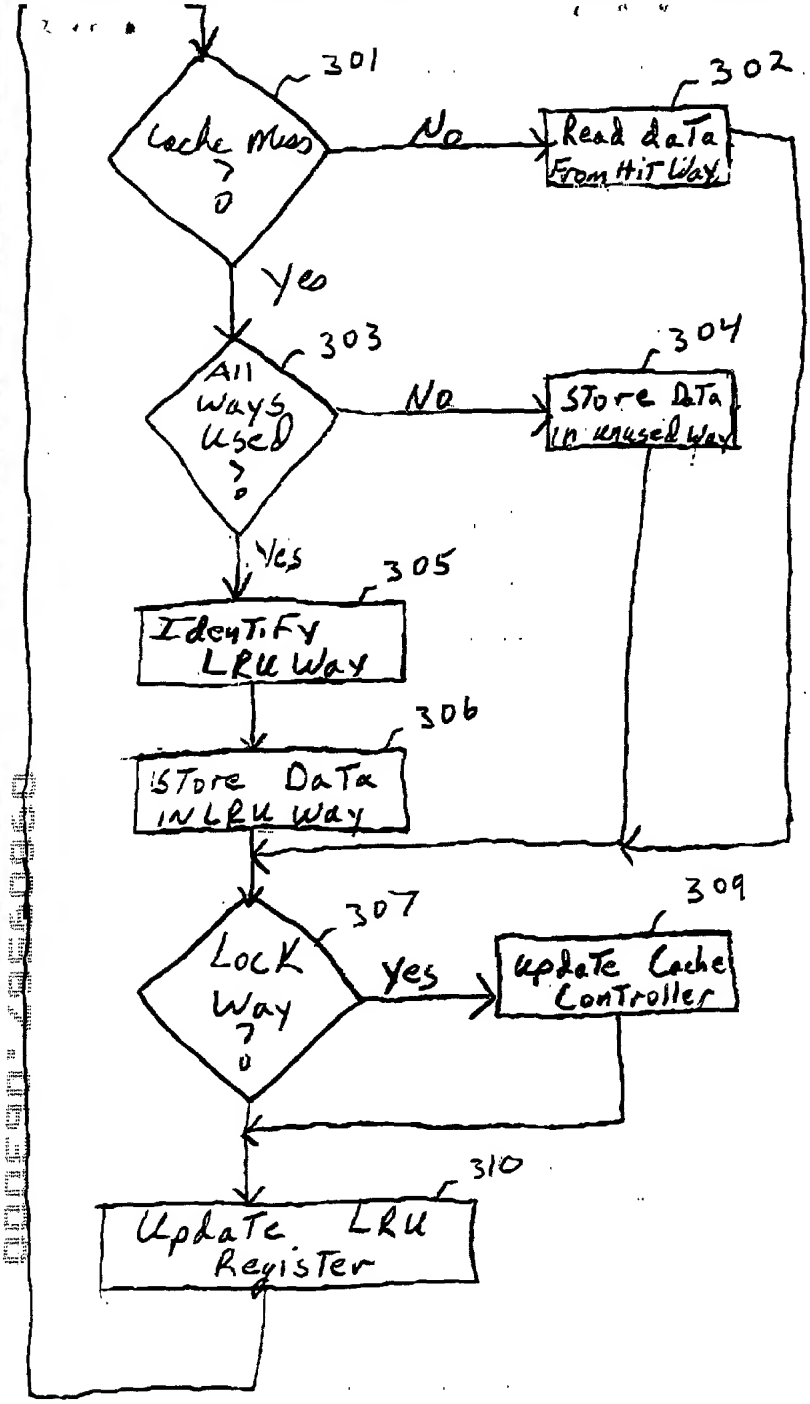

FIG. 3

42390.P9220

Bateman

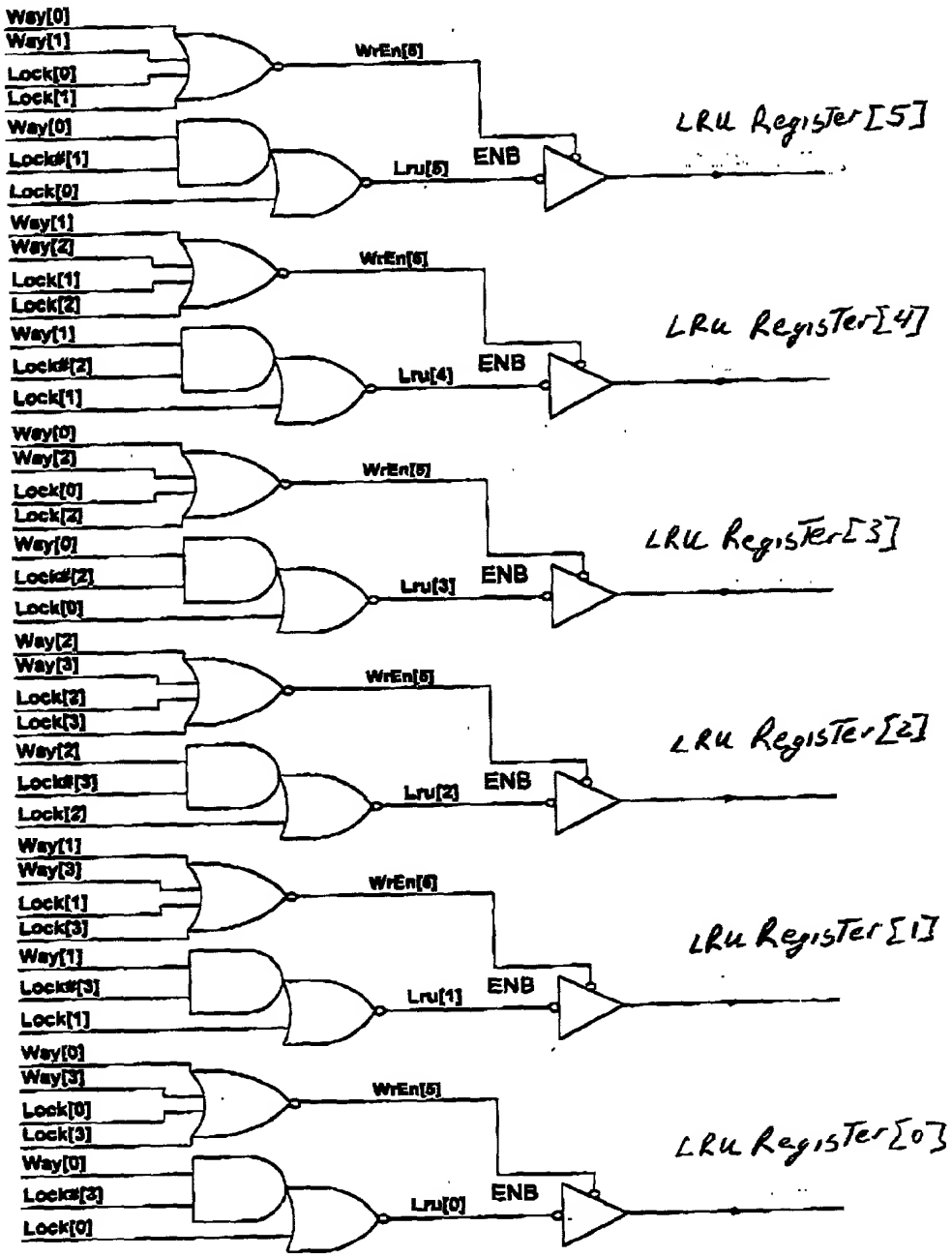

FIG. 4

42390.P9220
Bateman

(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CACHE HAVING A PRIORITIZED REPLACEMENT TECHNIQUE AND METHOD THEREFOR

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
Kenneth M. Seddon, Reg. No. 43,105, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
Kenneth M. Seddon, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Robert D. Bateman**

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

_____

APPENDIX A

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; Amy M. Armstrong, Reg. No. 42,265; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; George L. Fountain, Reg. No. 36,374; Paramita Ghosh, Reg. No. 42,806; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; Joseph Lutz, Reg. No. 43,765; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Darren J. Milliken, Reg. No. 42,004; Chun M. Ng, Reg. No. 36878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Lisa A. Norris, Reg. No. 44,976; Daniel E. Ovanezian, Reg. No. 41,236; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; James M. Wu, Reg. No. 45,241; Steven D. Yates, Reg. No. 42,242; and Norman Zafman, Reg. No. 26,250; my attorneys; and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; and John F. Travis, Reg. No. 43,203; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; John N. Greaves, Reg. No. 40,362; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. 44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.